



WINSTAR Display Co.,Ltd.
華凌光電股份有限公司



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SPECIFICATION

MODULE NO.:

WO12864C2

General Specification

Item	Dimension	Unit
Number of Dots	128 x 64 dots	—
Module dimension	55.2x 39.8 x 6.0	mm
View area	45.2 x 27.0	mm
Active area	40.92 x 24.28	mm
Dot size	0.28 x 0.34	mm
Dot pitch	0.32 x 0.38	mm
Duty	1/64 , 1/9 Bias	
Backlight Type	LED	
IC	ST7565P	
Interface	6800/8080/4-Line SPI	

Absolute Maximum Ratings

Item	Symbol	Min	Typ	Max	Unit
Operating Temperature	T _{OP}	-20	—	+70	°C
Storage Temperature	T _{ST}	-30	—	+80	°C
Power Supply Voltage	V _{DD}	-0.3	—	3.6	V
Power supply voltage (VDD standard)	V ₀ , V _{OUT}	-0.3	—	14.5	V
Power supply voltage (VDD standard)	V ₁ , V ₂ , V ₃ , V ₄	-0.3	—	V ₀ +0.3	V

Electrical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage For Logic	V _{DD} -V _{SS}	—	2.7	3.0	3.3	V
Supply Voltage For LCM	V _{OP}	T _a =-20°C	—	—	—	V
		T _a =25°C	9.4	9.6	9.8	V
		T _a =70°C	—	—	—	V
Input High Volt.	V _{IH}	—	0.8 V _{DD}	—	V _{DD}	V
Input Low Volt.	V _{IL}	—	V _{SS}	—	0.2 V _{DD}	V
Output High Volt.	V _{OH}	—	0.8 V _{DD}	—	V _{DD}	V
Output Low Volt.	V _{OL}	—	V _{SS}	—	0.2V _{DD}	V
Supply Current (No include LED Backlight)	I _{DD}	V _{DD} =3.0V	—	0.49	1.0	mA

Interface Pin Function

Pin No.	Symbol	Level	Description															
1	IRS	I	This terminal selects the resistors for the V0 voltage level adjustment. IRS = “H”: Use the internal resistors IRS = “L”: Do not use the internal resistors. The V0 voltage level is regulated by an external resistive voltage divider attached to the VR terminal															
2	/HPM	I	This is the power control terminal for the power supply circuit for liquid crystal drive. /HPM = “H”: Normal mode /HPM = “L”: High power mode (Default)															
3	P/S	I	This is the parallel data input/serial data input switch terminal. P/S = “H”: Parallel data input. P/S = “L”: Serial data input. The following applies depending on the P/S status: <table><tr><th>P/S</th><th>Data/Command</th><th>Data</th><th>Read/Write</th><th>Serial Clock</th></tr><tr><td>“H”</td><td>A0</td><td>D0 to D7</td><td>/RD, /WR</td><td>X</td></tr><tr><td>“L ”</td><td>A0</td><td>SI (D7)</td><td>Write only</td><td>SCL (D6)</td></tr></table> When P/S = “L”, D0 to D5 fixed “H”. /RD (E) and /WR (R/W) are fixed to either “H” or “L”. With serial data input, It is impossible read data from RAM	P/S	Data/Command	Data	Read/Write	Serial Clock	“H”	A0	D0 to D7	/RD, /WR	X	“L ”	A0	SI (D7)	Write only	SCL (D6)
P/S	Data/Command	Data	Read/Write	Serial Clock														
“H”	A0	D0 to D7	/RD, /WR	X														
“L ”	A0	SI (D7)	Write only	SCL (D6)														
4	C86	I	This is the MPU interface selection pin. C86 = “H”: 6800 Series MPU interface. C86 = “L”: 8080 Series MPU interface															
5	VR	I	Output voltage regulator terminal. Provides the voltage between VSS and V0 through a resistive voltage divider. IRS = “L” : the V0 voltage regulator internal resistors are not used. IRS = “H” : the V0 voltage regulator internal resistors are used.															
6~10	V0~V4	Power Supply	This is a multi-level power supply for the liquid crystal drive.															
11	VRS	Power Supply	This is the internal-output VREG power supply for the LCD power supply voltage regulator.															
12	CAP4+	O	DC/DC voltage converter.															
13	CAP2-	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2P terminal.															

14	CAP2+	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2N terminal.
15	CAP1+	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1N terminal.
16	CAP1-	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1P terminal.
17	CAP3+	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1N terminal.
18	CAP5+	O	DC/DC voltage converter.
19	VOUT	O	DC/DC voltage converter. Connect a capacitor between this terminal and vss or VDD
20	VSS	Power Supply	Ground
21	VDD	Power Supply	Power supply
22~29	D7~D0	I/O	Data bus line
30	/RD(E)	I	- When connected to 8080 series MPU, this pin is treated as the “/RD” signal of the 8080 MPU and is LOW-active. The data bus is in an output status when this signal is “L”. - When connected to 6800 series MPU, this pin is treated as the “E” signal of the 6800 MPU and is HIGH-active. This is the enable clock input terminal of the 6800 Series MPU.
31	/WR(R/W)	I	- When connected to 8080 series MPU, this pin is treated as the “/WR” signal of the 8080 MPU and is LOW-active. The signals on the data bus are latched at the rising edge of the /WR signal. - When connected to 6800 series MPU, this pin is treated as the “R/W” signal of the 6800 MPU and decides the access type : When R/W = “H”: Read. When R/W = “L”: Write.
32	A0	I	This is connect to the least significant bit of the normal MPU address bus, and it determines whether the data bits are data or command. A0 = “H”: Indicates that D0 to D7 are display data. A0 = “L”: Indicates that D0 to D7 are control data.
33	/RES	I	When RES is set to “L”, the setting are initialized.
34	/CS1	I	This is the chip select signal.

Contour Drawing

