



WINSTAR Display Co.,Ltd.
華凌光電股份有限公司



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SPECIFICATION

MODULE NO.: **WO240128B**

General Specification

Item	Dimension	Unit
Number of dots	240 x 128	—
Module dimension	122.2 x 79.8 x 6.5	mm
View area	114.0 x 64.0	mm
Active area	107.98 x 57.58	mm
Dot size	0.43 x 0.43	mm
Dot pitch	0.45 x 0.45	mm
Drive Method	1/128D , 1/12B	
Backlight Type	LED	
IC	ST7586S	
Interface	6800/8080/3 Line/4 Line	

Absolute Maximum Ratings

Item	Symbol	Min	Typ	Max	Unit
Operating Temperature	T _{OP}	-20	—	+70	°C
Storage Temperature	T _{ST}	-30	—	+80	°C
Digital Power Supply Voltage	V _{DDI}	-0.3	—	3.6	V
Analog Power supply voltage	V _{DDA}	-0.3	—	3.6	V
LCD Power supply voltage	V _{0-XV0}	-0.3	—	19	V
LCD Power supply voltage	V _G	-0.3	—	5.5	V

Electrical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage For Logic	V _{DD} -V _{SS}	—	3.0	3.3	3.6	V
Supply Voltage For LCM	V _{OP}	T _a =-20°C	—	—	—	V
		T _a =25°C	14.8	15.0	15.2	V
		T _a =+70°C	—	—	—	V
Input High Volt.	V _{IH}	—	0.7V _{DD}	—	V _{DD}	V
Input Low Volt.	V _{IL}	—	V _{ss}	—	0.3 V _{DD}	V
Output High Volt.	V _{OH}	—	0.8 V _{DD}	—	V _{DD}	V
Output Low Volt.	V _{OL}	—	V _{ss}	—	0.2V _{DD}	V
Supply Current	I _{DD}	V _{DD} =3.3V	—	2.0	4.0	mA

Interface Pin Function

Pin No.	Symbol	Description									
1	ESD GND	Electro-Static discharge									
2	VG	VG is the power of SEG-drivers									
3	XV0	Negative operating voltage of COM-drivers									
4	V0	Positive operating voltage of COM-drivers									
5	VM	VM is the non-select voltage level of COM-drivers									
6	VDDA	Power supply									
7	VSS	Ground									
8	VD1	Digital power source selection									
9	VDD1	VDD1 is the power of interface I/O circuit									
10	CSB	Chip select input pin CSB="L": This chip is selected and the MPU interface is active CSB="H": This chip is not selected and the MPU interface is disabled (D[7:0] are high impedance)									
11	IF3	These pins select interface operation mode									
12	IF2										
13	IF1	Note: Refer to "Interface Selection" for detailed information									
14	RSTB	Reset input pin. When RSTB is "L", internal initialization procedure is executed									
15	/RD(E)	Read / Write execution control pin. (This pin is only used in parallel interface) <table border="1"> <thead> <tr> <th>MPU Type</th> <th>ERD</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>6800-series</td> <td>E</td> <td>Read / Write control input pin. R/W = "H": When E is "H", data bus is in output status. R/W = "L": The data are latched at the falling edge of the E signal.</td> </tr> <tr> <td>8080-series</td> <td>/RD</td> <td>Read enable input pin. When /RD is "L", data bus is in output status.</td> </tr> </tbody> </table> <p>This pin is not used in serial interfaces and should be connected to VDD1</p>	MPU Type	ERD	Description	6800-series	E	Read / Write control input pin. R/W = "H": When E is "H", data bus is in output status. R/W = "L": The data are latched at the falling edge of the E signal.	8080-series	/RD	Read enable input pin. When /RD is "L", data bus is in output status.
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8080-series	/RD	Read enable input pin. When /RD is "L", data bus is in output status.									

16~23	D7~D0	<p>The bi-directional data bus of the MPU interface. When CSB is "H", they are high impedance</p> <p>If using serial interface:</p> <p>D0 is the SDA signal in 4-Line & 3-Line interface</p> <p>D1 is the A0 signal in 4-Line interface</p>									
24	/WR/(R/W)	<p>Read / Write execution control pin. (This pin is only used in parallel interface)</p> <table border="1"> <thead> <tr> <th>MPU Type</th> <th>RWR</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>6800-series</td> <td>R/W</td> <td> Read / Write control input pin R/W = "H" : read R/W = "L" : write </td> </tr> <tr> <td>8080-series</td> <td>/WR</td> <td> Write enable clock input pin. The data are latched at the rising edge of the /WR signal. </td> </tr> </tbody> </table> <p>This pin is not used in serial interfaces and should be connected to VDD1</p>	MPU Type	RWR	Description	6800-series	R/W	Read / Write control input pin R/W = "H" : read R/W = "L" : write	8080-series	/WR	Write enable clock input pin. The data are latched at the rising edge of the /WR signal.
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8080-series	/WR	Write enable clock input pin. The data are latched at the rising edge of the /WR signal.									
25	A0(SCL)	<p>The function of this pin is different in parallel and serial interface</p> <p>In parallel interface: A0 is register selection input</p> <p>A0 = "H": inputs on data bus are display data</p> <p>A0 = "L": inputs on data bus are command</p> <p>In serial interface: this pad will be used as SCL (serial-clock) input</p>									
26	ESD GND	Electro-Static discharge									

Contour Drawing

