### WINSTAR Display

# **OLED SPECIFICATION**

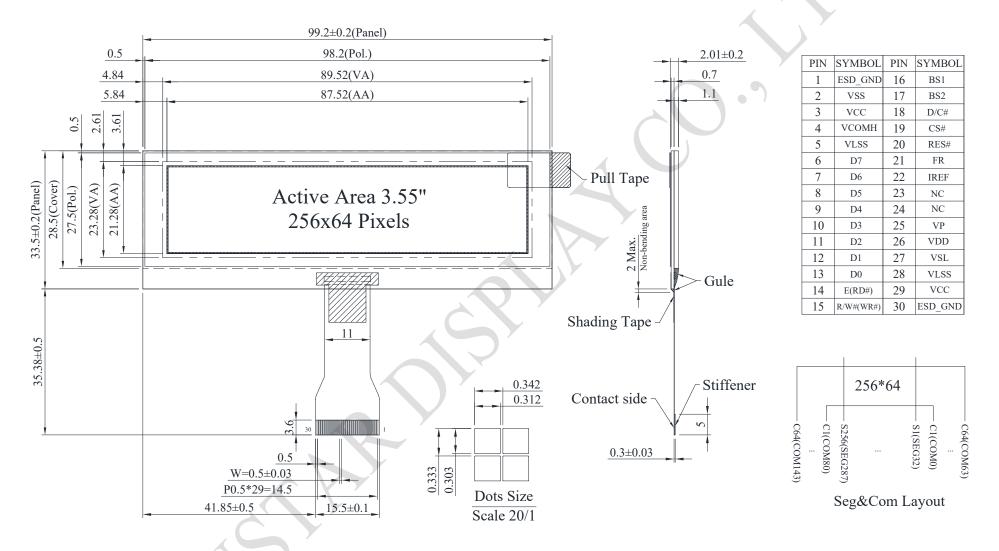
Model No:

WEO025664E

## **General Specification**

| Item             | Dimension                | Unit |  |  |  |
|------------------|--------------------------|------|--|--|--|
| Dot Matrix       | 256 x 64 Dots            | - ^  |  |  |  |
| Module dimension | 99.2 x 33.5 x 2.01       | mm   |  |  |  |
| Active Area      | 87.52 x 21.28            | mm   |  |  |  |
| Pixel Size       | 0.312 x 0.303            | mm   |  |  |  |
| Pixel Pitch      | 0.342 x 0.333            | mm   |  |  |  |
| Display Mode     | Passive Matrix           |      |  |  |  |
| Display Color    | Monochrome               |      |  |  |  |
| Drive Duty       | 1/64 Duty                |      |  |  |  |
| Gray Scale       | 4 bits                   |      |  |  |  |
| IC               | SSD1363                  |      |  |  |  |
| Interface        | 6800,8080,4-Wire SPI,I2C |      |  |  |  |
| Size             | 3.55 inch                |      |  |  |  |

#### **Contour Drawing & Block Diagram**



The non-specified tolerance of dimension is  $\pm 0.3$ mm.

### **Interface Pin Function**

| Pin<br>Number | Symbol         | Function   |  |  |  |
|---------------|----------------|--|--|--|--|
| 1             | ESD_GND        | ESD Ground pin   |  |  |  |
| 2             | VSS            | Ground pin. It must be connected to external ground.   |  |  |  |
| 3             | VCC            | Power supply for panel driving voltage. This is also the most positive power voltage supply pin.  A capacitor should be connected between this pin and VSS.  |  |  |  |
| 4             | VCOMH          | COM signal deselected voltage level. A capacitor should be connected between this pin and VSS.   |  |  |  |
| 5             | VLSS           | Analog system ground pin. It must be connected to external ground.   |  |  |  |
| 6<br>7<br>8   | D7<br>D6<br>D5 | These pins are bi-directional data bus connecting to the MCU data bus. Unused pins are recommended to tie LOW.   |  |  |  |
| 9             | D4             | When serial interface mode is selected, D2, D1 should be tied together as  |  |  |  |
| 10            | D3             | the serial data input: SDIN, and D0 will be the serial clock input: SCLK.  |  |  |  |
| 11            | D2             | When I2C mode is selected, D2, D1 should be tied together and serve as   |  |  |  |
| 12            | D1<br>D0       | SDAout, SDAin in application and D0 is the serial clock input, SCL.  |  |  |  |
| 14            | E(RD#)         | This pin is MCU interface input.  When 6800 interface mode is selected, this pin will be used as the Enable (E) signal.  Read/write operation is initiated when this pin is pulled HIGH and the chip is selected.  When 8080 interface mode is selected, this pin receives the Read (RD#) signal. Read operation is initiated when this pin is pulled LOW and the chip is selected.  When serial or I2C interface is selected, this pin must be connected to VSS.  |  |  |  |
| 15            | R/W#<br>(WR#)  | This pin is read / write control input pin connecting to the MCU interface. When 6800 interface mode is selected, this pin will be used as Read/Write (R/W#) selection input. Read mode will be carried out when this pin is pulled HIGH and write mode when LOW. When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled LOW and the chip is selected. When serial or I2C interface is selected, this pin must be connected to VSS. |  |  |  |

| BS1     | describe  | 8080  | I2C                             | 6800                                 | 4-wire SPI                                     |
|---------|---|---|---------------------------------|--------------------------------------|--|
|         | BS1   | 1   | 1                               | 0                                    | 0  |
|         | BS2   | 1   | 0                               | 1                                    | 0  |
| BS2     |   |   |                                 |                                      |  |
| D/C#    | When th<br>When th<br>comman  | e pin is pulled<br>e pin is pulled<br>d register.   | HIGH, the data<br>LOW, the data | a at D[7:0] will<br>at D[7:0] will b | be interpreted as data.<br>se transferred to a |
| CS#     | This pin is the chip select input connecting to the MCU.  The chip is enabled for MCU communication only when CS# is pulled LOW   |   |                                 |                                      |  |
| RES#    | This pin is reset signal input. When the pin is pulled LOW, initialization of the chip is executed.   |   |                                 |                                      |  |
| FR      | This pin outputs RAM write synchronization signal. Proper timing between MCU data writing and frame display timing can be achieved to prevent tearing effect.   |   |                                 |                                      |  |
| IREF    | This pin is the segment output current reference pin. IREF is supplied externally. A resistor should be connected between this pin and VSS to maintain the current around 10uA. It should be kept floating when internal IREF is chosen by command setting. |   |                                 |                                      |  |
| NC      | This is d   | ummy pin. It s  | hould be kept N                 | NC.                                  |  |
| VP      | This pin is the segment pre-charge voltage reference pin.  A capacitor can be connected between this pin and VSS to improve visual performance. It can also be float per application.  No external power supply is allowed to connect to this pin.          |   |                                 |                                      |  |
| VDD     | Power supply pin for core logic operation. A capacitor should be connected between this pin and VSS.  |   |                                 |                                      |  |
| VSL     | This is segment voltage (output low level) reference pin. This pin has to be connected with resistor and diode to ground (details depends on application).  |   |                                 |                                      |  |
| VLSS    | Analog s  | ystem ground  | pin. It must be                 | connected to                         | external ground.                               |
| VCC     | Power supply for panel driving voltage. This is also the most positive power voltage supply pin.  A capacitor should be connected between this pin and VSS.   |   |                                 |                                      |  |
| ESD_GND | ESD Gro   | ound pin  |                                 |                                      |  |
|         | D/C#  CS#  RES#  FR  IREF  NC  VP  VDD  VSL  VLSS  VCC  | BS1  BS2  Note: (1) 0 is c (2) 1 is c (2) 1 is c (3) 1 is c (4) 1 is c (5) 1 is c (6) 1 is c (7) 2 is c (8) 1 is c (9) 1 is c (1) 0 is c (1) 0 is c (2) 1 is c (2) 1 is c (3) 1 is c (4) 1 is c (5) 1 is c (7) 1 is pin (8) 1 is pin (9) 1 is c (1) 0 is c (1) 0 is c (1) 0 is c (1) 0 is c (2) 1 is c (1) 0 is c (1) 0 is c (1) 0 is c (2) 1 is c (1) 0 is c (2) 1 is c (1) 0 is c (1) is c (1) 0 is c (1) is c (1) 0 | BS1    BS2                      | BS1    BS2   1   0                   | BS1  |

### **Absolute Maximum Ratings**

| Parameter             | Symbol | Min  | Max  | Unit |
|-----------------------|--------|------|------|------|
| Supply Voltage        | VDD    | -0.3 | 4.0  | V    |
| Supply Voltage        | VCC    | -0.5 | 19.0 | V    |
| Operating Temperature | TOP    | -40  | +80  | °C   |
| Storage Temperature   | TSTG   | -40  | +85  | °C   |

### **Electrical Characteristics**

#### **DC Electrical Characteristics**

| Item  | Symbol | Condition | Min     | Тур  | Max     | Unit |
|---|--------|-----------|---------|------|---------|------|
| Low voltage power supply, power Supply for I/O pins | VDD    | <u></u>   | 1.65    | 3.0  | 3.3     | V    |
| Operating Voltage                                   | VCC    |           | 8.0     | 16.0 | 16.5    | V    |
| High Level Input                                    | VIH    |           | 0.8×VDD | _    | VDD     | V    |
| Low Level Input                                     | VIL    | _         | 0       | _    | 0.2×VDD | V    |
| High Level Output                                   | VOH    | _         | 0.9×VDD | _    | VDD     | V    |
| Low Level Output                                    | VOL    | _         | 0       |      | 0.1×VDD | V    |
| Display 50% Pixel on                                | ICC    | VCC =16V  | _       | 30   | 45      | mA   |

**NATURE**